**Assignment-7 Verilog Part-3**

**Group: 10**

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**For simulation:**

The Verilog code consists of three main modules. The testbench calls the mainmodule which makes calls to the register bank to fetch the values in the registers given a particular register number when the read signal is turned on and writes a value into a particular register when the write signal is 1. This module also makes calls to the ALU module after fetching the register values from the register bank and then obtains the result from the ALU module and writes it back into the respective register through the register bank module.

**For synthesis:**

This contains an additional fpga module to fetch the values from the fpga board for all the inputs, rs (the source register number), rt (second source register number), imm (immediate value), rd (final destination register), opcode (the operation code for the operation to be done). Thid module then makes call to the above implemented mainmodule. Then the execution is same as above.